

LEGW35T120HA1

IGBT Chip

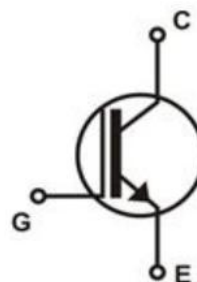
Features:

- Trench & Field Stop technology
- Low Vcesat
- Positive Vcesat temperature coefficient
- Low turn-off losses
- Short tail current
- Easy paralleling

V_{CE}	1200V
I_c	35A
Die Size	5.704mm × 6.3707mm

Applications:

- The inverter



G: gate C: collector E: emitter

Internal Circuit

Mechanical Parameters

Parameter	Value
Die Size	5.704mm × 6.3707mm
Scirbe line	80μm
Gate Pad Size	1.104mm × 0.731mm
Wafer Size	200mm
Wafer Thickness	130μm
Max. possible chips per wafer	700
Front side Metal	Al /Cu, 4μm
Backside Metal	Al / Ti/ Ni / Ag

Maximum Ratings

Symbol	Description	Value	Unit
V_{CE}	Collector-Emitter Voltage, $T_j = 25^\circ\text{C}$	1200	V
I_C	DC Collector Current, Limited By $T_{jmax.}$	35 ¹⁾	A
$I_{C, puls}$	Pulsed Collector Current, tp Limited By $T_{jmax.}$	105	A
V_{GE}	Gate Emitter Voltage	± 20	V
T_{vj}	Junction Temperature Range	$-40....+175$	$^\circ\text{C}$
T_{jr}, T_{stg}	Operating Junction And Storage Temperature	$-55....+150$	$^\circ\text{C}$
tsc	Short Circuit Data $V_{GE} = 15\text{V}, V_{CC} = 600\text{V}, T_j = 150^\circ\text{C}$	10 ¹⁾	μs
RBSOA	Reverse Bias Safe Operating Area ²⁾	$I_{C, max} = 70\text{A}, V_{CE, max} = 1200\text{V}, T_{vj} \leq 150^\circ\text{C}$	

1) depending on Leading Energy L1 package

2) Not subject to production test - verified by design/characterization

Static Characteristics ($T_j = 25^\circ\text{C}$, unless otherwise specified) ¹⁾

Symbol	Description	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)CES}$	Collector-Emitter breakdown voltage	$V_{GE}=0\text{V}, I_C = 1\text{mA}$	1200	-	-	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$V_{GE} = 15\text{V}, I_C = 35\text{A}$	1.7	1.85	2.3	V
$V_{GE(th)}$	Gate Threshold Voltage	$V_{CE} = V_{GE}, I_C = 2\text{mA}$	5.0	6.2	6.5	V
I_{CES}	Collector-Emitter Cut-off Current	$V_{CE} = 1200\text{V}, V_{GE} = 0\text{V}$	-	-	20	μA
I_{GES}	Gate - Emitter Leakage Current	$V_{CE} = 0\text{V}, V_{GE} = 20\text{V}$	-	-	200	nA
r_G	Integrated gate resister		-	TBD	-	Ω
C_{ies}	Input Capacitance	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHZ}$	-	3.11	-	nF
C_{oes}	Output Capacitance		-	138	-	pF
C_{res}	Reverse Transfer Capacitance		-	103	-	pF

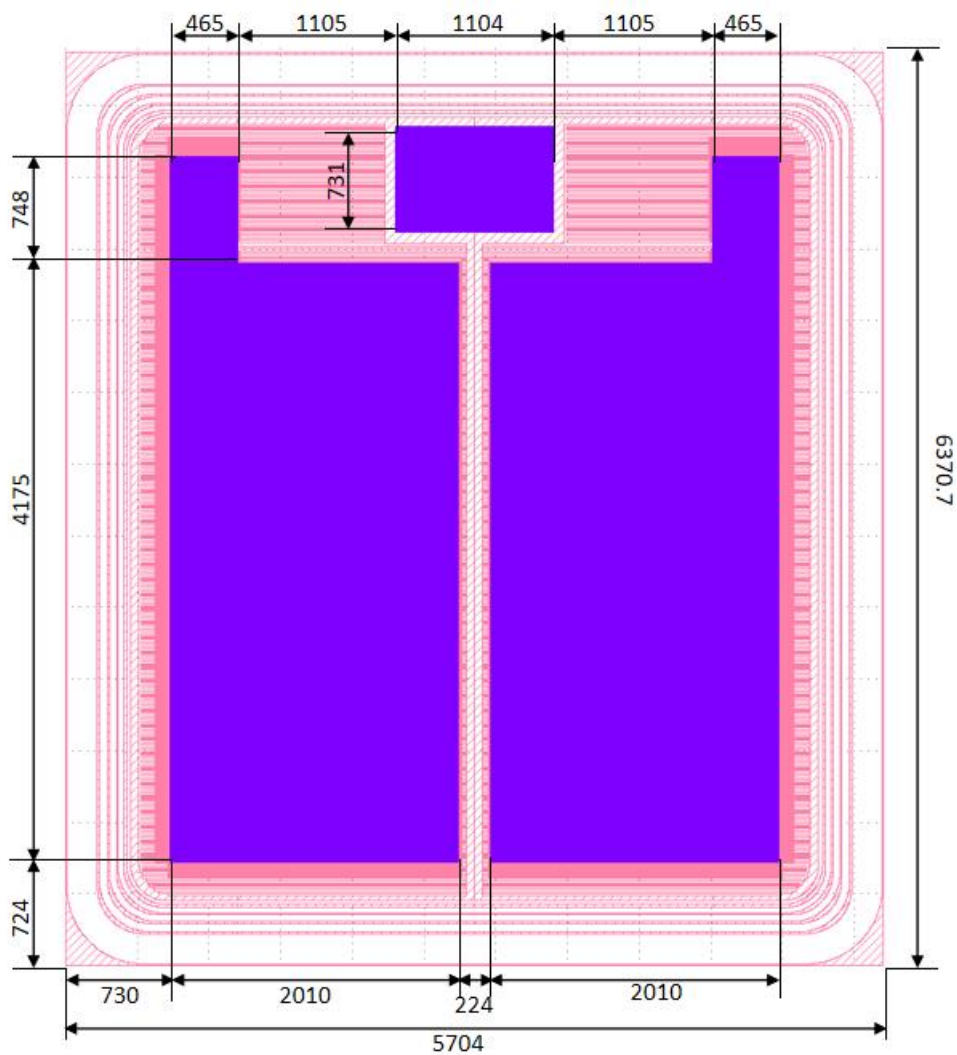
1) depending on Leading Energy L1 package

Dynamic Characteristics ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise specified) ¹⁾

Symbol	Description	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$t_{d(on)}$	Turn-on Delay Time	$I_C = 35\text{ A}, V_{CE} = 600\text{ V}$ $V_{GE} = \pm 15\text{ V}$ $R_{Gon} = 15\Omega$ $T_{vj} = 25\text{ }^{\circ}\text{C}$		50	-	ns
t_r	Rise Time			48	-	ns
$t_{d(off)}$	Turn-off Delay Time			200	-	ns
t_f	Fall TimeLeakage Current			156	-	ns
Eon	Turn-on Switching Loss			2.64	-	mJ
Eoff	Turn-off Switching Loss			1.87	-	mJ
$t_{d(on)}$	Turn-on Delay Time	$I_C = 35\text{ A}, V_{CE} = 600\text{ V}$ $V_{GE} = \pm 15\text{ V}$ $R_{Gon} = 15\Omega$ $T_{vj} = 125\text{ }^{\circ}\text{C}$		55	-	ns
t_r	Rise Time			60	-	ns
$t_{d(off)}$	Turn-off Delay Time			240	-	ns
t_f	Fall TimeLeakage Current			240	-	ns
Eon	Turn-on Switching Loss			3.22	-	mJ
Eoff	Turn-off Switching Loss			3.01	-	mJ

1) depending on Leading Energy L1 package

Chip Drawing (Dimensions: μm)



DISCLAIMER

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE
TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE