LEGW50T120SA1

IGBT Chip

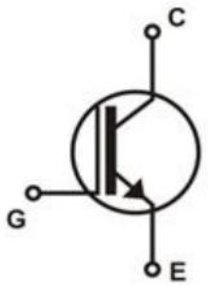
Features:

- Trench & Field Stop technology
- Low Vcesat
- Positive Vcesat temperature coefficient
- Low turn-off losses
- Short tail current
- Easy paralleling

V_{CE}	1200V
I_C	50A
Die Size	7.5845mm ×7.5147mm

Applications:

- The inverter
- Inductive heating
- Electronic welder



G：gate C：collector E：emitter

Internal Circuit

Mechanical Parameters

Parameter	Value
Die Size	7.5845mm ×7.5147mm
Scirbe line	80μm
Gate Pad Size	1.214mm × 0.639mm
Wafer Size	200mm
Wafer Thickness	130μm
Max. possible chips per wafer	431
Front side Metal	Al /Cu, 4μm
Backside Metal	Al / Ti/ Ni / Ag

Maximum Ratings

Symbol	Description	Value	Unit
V_{CE}	Collector-Emitter Voltage, T_j = 25℃	1200	V
I_C	DC Collector Current, Limited By $T_{jmax.}$	50 1)	A
$I_{c,\ puls}$	Pulsed Collector Current, tp Limited By $T_{jmax.}$	150	A
V_{GE}	Gate Emitter Voltage	±20	V
T_{vj}	Junction Temperature Range	-40....+175	℃
T_j, T_{stg}	Operating Junction And Storage Temperature	-40....+150	℃
tsc	Short Circuit Data V_{GE} = 15V,V_{CC} = 600V,T_j =150℃	10 1)	us
RBSOA	Reverse Bias Safe Operating Area 2)	$I_{C,\ max}$ = 100A, $V_{CE,\ max}$ = 1200V, T_{vj} ≤ 150℃	

1) depending on Leading Energy L1 package

2) Not subject to production test - verified by design/characterization

Static Characteristics (T_j= 25 ℃, unless otherwise specified) 1)

Symbol	Description	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{(BR)CES}$	Collector-Emitter breakdown voltage	VGE=0V , IC= 1mA	1200	-	-	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	V_{GE} = 15V, I_C = 50A	1.7	2.05	2.5	V
$V_{GE(th)}$	Gate Threshold Voltage	V_{CE} = V_{GE}, I_C = 2mA	5.0	6.2	6.5	V
I_{CES}	Collector-Emitter Cut-off Current	V_{CE} = 1200V, V_{GE}= 0V	-	-	20	μA
I_{GES}	Gate - Emitter Leakage Current	V_{CE} = 0V, V_{GE} = 20V	-	-	200	nA
r_G	Integrated gate resister		-	TBD	-	Ω
C_{ies}	Input Capacitance	V_{CE} = 25V, V_{GE} = 0V, f = 1MHZ	-	TBD	-	pF
C_{oes}	Output Capacitance		-	TBD	-	pF
C_{res}	Reverse Transfer Capacitance		-	TBD	-	pF

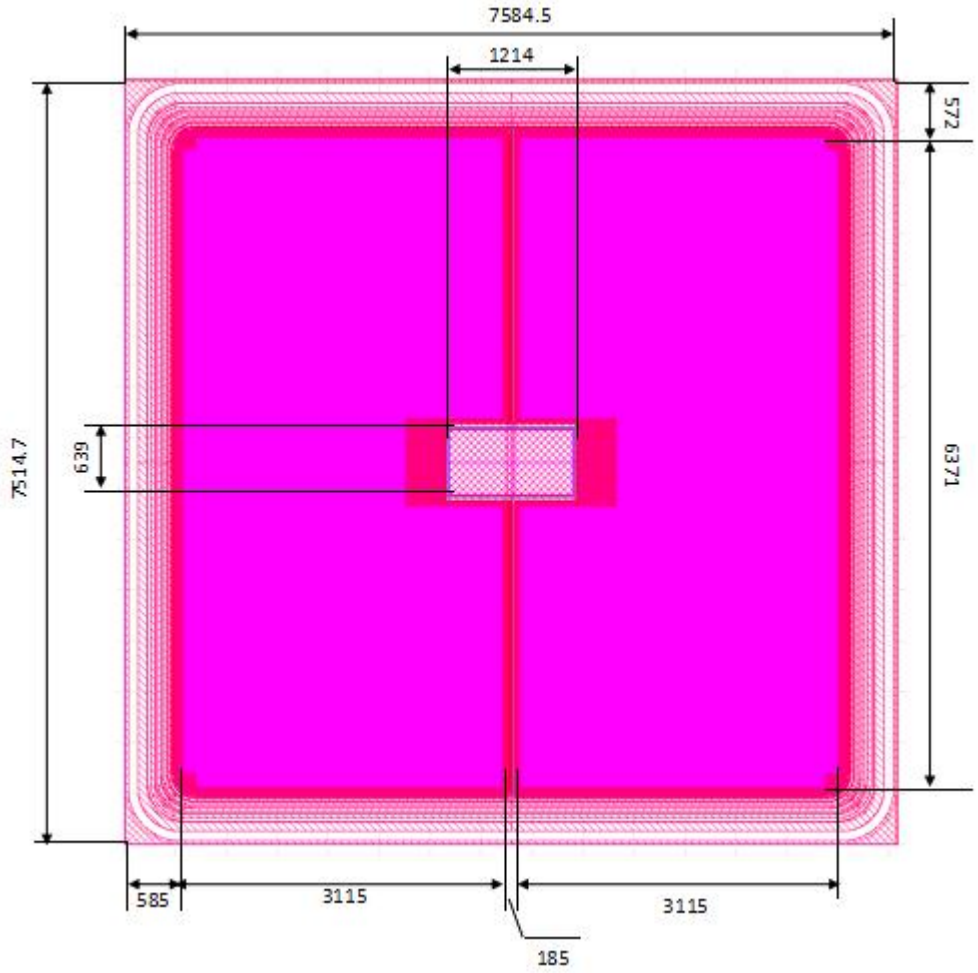
1) depending on Leading Energy L1 package

Dynamic Characteristics (T_j= 25 ℃, unless otherwise specified) 1)

Symbol	Description	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$t_{d(on)}$	Turn-on Delay Time	I_C=50 A,V_{CE}=600 V V_{GE}=±15 V R_{Gon}=15 Ω T_j=25 ℃	-	130	-	ns
t_r	Rise Time		-	100	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	310	-	ns
t_f	Fall TimeLeakage Current		-	100	-	ns
Eon	Turn-on Switching Loss		-	5.5	-	mJ
Eoff	Turn-off Switching Loss		-	2.6	-	mJ
$t_{d(on)}$	Turn-on Delay Time	I_C=50 A,V_{CE}=600 V V_{GE}=±15 V R_{Gon}=15 Ω T_j=150 ℃	-	130	-	ns
t_r	Rise Time		-	110	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	350	-	ns
t_f	Fall TimeLeakage Current		-	180	-	ns
Eon	Turn-on Switching Loss		-	7.2	-	mJ
Eoff	Turn-off Switching Loss		-	3.7	-	mJ

1) depending on Leading Energy LT package

Chip Drawing (Dimensions: μm)



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